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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/911,851	07/25/2001	Hak Su Kim	CIT/K-152	3915

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EXAMINER	
LESPERANCE, JEAN E	

ART UNIT	PAPER NUMBER
2674	12

DATE MAILED: 01/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/911,851	KIM, HAK SU	
	Examiner	Art Unit	
	Jean E Lesperance	2674	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 September 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 8-20* is/are rejected.

7)☒ Claim(s) *4-6* is/are objected to.

8)☒ Claim(s) *7* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 July 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

Group I. Claims 1-6 and 8-20, drawn to a display driving control circuit, classified in class 345, subclass 204.

Group II. Claim 7, drawn to a reactive power control, classified in class 323, subclass 205.

The inventions are distinct, each from the other because:

Group I which is a display driving control circuit is functional on its own and does not need Group I. Group II which is a reactive power control can function independently from Group I.

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

During a telephone conversation with Daniel Kim on 1-14-2004 a provisional election was made with traverse to prosecute the invention of Group I, claims 1-6 and 8-20. Affirmation of this election must be made by applicant in replying to this Office action. Claim 7 withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

2. Claims 1-6 and 8-20 are presented for examination.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3 are rejected under 35 U.S.C. 103 (a) as being unpatentable over U.S. Patent # 5,532,712 ("Tsuda et al.").

As for claim 1, Tsuda et al. teach a Vcc connected to the shift register acting as a power supply (Fig.8) corresponding to a DC-DC converter provided inside one chip, for controlling an external voltage input depending on a timing control signal and providing a controlled DC voltage; the PC terminal is connected through an inverter 3c to a first input of each of the plurality of gate circuits 2b (column 6, lines 64-66) corresponding to an interface unit provided inside the chip, for interface with parts outside the chip; shift register Fig.8 (3a) corresponding to a memory provided inside the chip, for storing display information transmitted through the interface unit: latch Fig.8 (3b) corresponding to a data processor provided inside the chip, for providing a display data to a display panel of the EL display device using the display information stored in the memory and the controlled DC voltage output from the DC-Dc converter; a plurality of first gate circuits 2a and a plurality of second gate circuits 2b (Fig.8) corresponding to a scan processor provided inside the chip, for outputting scan data to the display panel using

the display information and the controlled DC-voltage output from the DC-DC converter: and the clock terminal connected to the latch 6b and through an inverter 3e to the shift register 3a (column 7, lines 38-39) corresponding to a timing control unit provided inside the chip, for providing the timing control signal to the DC-DC converter, the interface unit, the memory, the data processor, and the scan processor. The prior art does not explicitly teach a DC-DC provided inside the chip acting as a power supply for controlling the external voltage. However, the prior teaches a power supply Vcc connected to shift register inside the chip acting as a power supply.

Thus, it would have been obvious to a person of ordinary skill in the art to modify the DC-DC converter to achieve the Vcc connected to the shift register inside the chip because this would provide a drive circuit, for use with a transmission scattered liquid display device, which allows an image to be quickly changed without the occurrence of a residual image.

As for claim 2, Tsuda et al. teach a power supply terminal not shown in Fig.12, a positive voltage +V as a signal Vdd2 is supplied to a first terminal of the switch SW1 (column 10, lines 15-17) corresponding to power peripheral unit provided outside the chip, for controlling input and output voltages of the DC-DC converter, preventing a backward current from occurring during the DC-DC conversion, and maintaining the input DC voltage for a predetermined-time.

As for claim 3, Tsuda et al. teach an insulated DC-DC converter (Fig.10) where it is inherent to include an inductor, a diode, and a resistor.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 8-12 are rejected under 35 U.S.C. 102 (b) as being unpatentable over U.S. Patent # 5,489,867 ("Tamanoi").

As for claim 8, Tamanoi teaches some voltage converters 22.sub.1 to 22.sub.n Fig.5 corresponding to a voltage converter; and a display data driving integrated circuit (IC) for driving a matrix display unit, and more particularly to a control circuit for controlling the operation timing relationship between the groups of display driving signal output driving buffer circuits corresponding to circuitry configured to drive a display device.

As for claim 9, Tamanoi teaches The voltage converter circuits 22.sub.1 to 22.sub.n convert the outputs of the 64 EXCLUSIVE-OR circuits 19.sub.1 to 19.sub.n into specific high-voltage levels and output the converted levels through push-pull driving circuits (not shown), thus supplying output signals OUT.sub.1 to OUT.sub.n for 64 bits as a dynamic driving signals to a matrix liquid-crystal display unit (not shown) via output terminals 23.sub.1 to 23.sub.n for 64 bits (column 4, lines 46-54) corresponding to the Vcc connected to the shift register (3a) is from probably a step down voltage because the shift register can only accept a certain level of power supply corresponding to a the voltage converter is a direct current to direct current voltage

converter because the from the wall AC the voltage is converted to DC which has to be further converted to or step down to the level of voltage that the components can accept.

As for claim 10, Tamanoi teaches some exclusive OR Fig.5 (19) corresponding to a scan processor and some AND gate Fig.5 (16) corresponding to a data processor.

As for claim 11, Tamanoi teaches the driving buffer circuits 24 which is an integrated circuit (Fig.5) corresponding to the integrated circuit is comprised on a chip.

As for claim 12, Tamanoi teaches a control circuit for controlling the operation timing relationship between the groups of display driving signal output driving buffer circuits (column 1, lines 11-13) corresponding to wherein the voltage converter comprises a voltage control unit.

Claims 13-20 are rejected under 35 U.S.C. 103 (a) as being unpatentable over U.S. Patent # 5,489,867 ("Tamanoi").

As for claim 13-17, Tamanoi teaches the voltage converter circuits 22.sub.1 to 22.sub.n convert the outputs of the 64 EXCLUSIVE-OR circuits 19.sub.1 to 19.sub.n into specific high-voltage levels and output the converted levels through push-pull driving circuits (not shown), thus supplying output signals OUT.sub.1 to OUT.sub.n for 64 bits as a dynamic driving signals to a matrix liquid-crystal display unit (not shown) via output terminals 23.sub.1 to 23.sub.n for 64 bits (column 4, lines 46-54) corresponding to the voltage control unit is configured to vary impedance to control the level of an output voltage, apparatus comprises an impedance generating unit, the impedance generating unit is configured to transmit a control signal to the voltage

control unit to vary the impedance of the voltage control unit, the impedance generating unit is comprised in the integrated circuit, and the impedance generating unit is external to the integrated circuit. The prior art odes not explicitly teaches the impedance generating unit and the control unit to vary it. However, the prior are teaches the push-pull driving circuits thus supplying output signals out1 to out-n.

Thus, it would have been obvious to a person skill in the art to modify the push-pull driving circuits thus supplying output signals out1 to out-n to achieve the impedance generating unit and the control unit to vary it because this would provide a display data driving IC capable of not only suppressing the switching current in the multitude channel driving buffer circuits, but also improving the quality of tone display when a multi-tone display unit is driven.

As for claims 18-20,Tamanoi teaches a control circuit for controlling the operation timing relationship between the groups of display driving signal output driving buffer circuits (column 1, lines 11-13) corresponding to the voltage control unit comprises: anf the input terminal, the output terminal and the feedback terminal are inherent in the control circuit; it is also inherent that the inductor is coupled between the input terminal and the output terminal and a diode and a resistor are coupled in series between the output terminal and the feedback terminal within the control circuit.

Allowable Subject Matter

4. Claims 4 and 5 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Reasons for allowance

5. The following is an examiner's statement of reasons for allowance:

None of the references either singularly or in combination, teaches or fairly suggests: The driving circuit for an orqanic EL device, wherein the power peripheral unit includes: an input terminal providing an applying external voltage an external voltage to the DC-DC converter; an output terminal output terminal outputting the controlled DC voltage output from the DC-DC converter to the outside the chip; a first capacitor connected with the input terminal in parallel to minimize fluctuation of the input voltage; a second capacitor connected with the output terminal in parallel to minimize fluctuation of the controlled DC voltage; an inductor connected in series between the input terminal and the output terminal, for maintaining the external voltage applied to the DC-DC converter for a predetermined time; and a diode connected in series between the input terminal and the output terminal, for preventing a backward current from occurring.

The closest arts, Tamanoi and Tsuda et al. as discussed above, either singularly or in combination, fail to anticipate or render the above underlined limitations obvious.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jean Lesperance whose telephone number is (703)

308-6413. The examiner can normally be reached on from Monday to Friday between 8:OOAM and 4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Hjerpe, can be reached on (703) 305-4709 .

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

Jean Lesperance

Art Unit 2674

Date 1-15-2004

RICHARD HJERPE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600